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Table of Contents

Note : Remove "Table of Content" before including in CP Book
Each Course Plan shall be printed and made into a book with cover page
Blooms Level in all sections match with A.2, only if you plan to teach / learn at higher levels

3. 18CS34: Computer Organization

A. COURSE INFORMATION

1. Course Overview

Degree:	BE	Program:	CS
Year / Semester :	3	Academic Year:	2018-19
Course Title:	Computer Organization	Course Code:	18CS34
Credit / L-T-P:	4-0-0	SEE Duration:	180 Minutes
Total Contact Hours:	50	SEE Marks:	75 Marks
CIA Marks:	40	Assignment	1 / Module
Course Plan Author:	Sowmya C V	Sign	Dt:
Checked By:		Sign	Dt:

2. Course Content

Module	Module Content	Teaching Hours	Module Concepts	Blooms Level
1	Basic operational Concepts, Bus Structures, Processor clock, Basic Performance Equation, Clock Rate, Performance Measurement, Memory Location and Addresses, Memory Operations, Instructions and Instruction Sequencing, Addressing Modes, Assembly Language, Basic Input and Output Operations, Stacks and Queues, Subroutines, Additional Instructions, Encoding of Machine Instructions	10	Computer Organization and Machine instructions structure	L2, L4
2	Accessing I/O Devices, interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Controlling Device Requests, Exceptions, Direct Memory Access, Buses, Buses, Interface Circuits, PCI Bus, SCSI Bus, USB	10	Input output organization and interrupts and Standard input output interfaces	L2
3	Basic Concepts, Semiconductor RAM Memories, Read Only Memories, Speed, Size, and Cost, Cache Memories – Mapping Functions, Replacement Algorithms, Performance Considerations, Virtual Memories, Secondary Storage	10	Memory System and storage devices	L2, L4
4	Numbers, Arithmetic Operations and Characters, Addition and Subtraction of Signed Numbers, Design of Fast Adders, Numbers, Arithmetic Operations and Characters, Addition and Subtraction of Signed Numbers, Design of Fast Adders	10	Arithmetic Operations and Binary operations	L2,L3
5	Some Fundamental Concepts, Execution of a Complete Instruction, Multiple Bus Organization, Hard-wired Control, Micro programmed Control, Examples of embedded Systems, Processor chips for embedded applications, Simple Micro controller, The structure of General-Purpose Multiprocessors	10	Processing unit and Embedded system and large computer system	L2

3. Course Material

Module	Details	Available
1	Text books	
	1. Carl Hamacher, Zvonko Vranesic, Safwat Zaky: Computer Organization, 5th Edition, Tata McGraw Hill,2002.	In Lib
2	Reference books	
	1. William Stallings: Computer Organization & Architecture, 9 th Edition, Pearson, 2015.	In dept
3	Others (Web, Video, Simulation, Notes etc.)	
	https://www.youtube.com/watch?v=v4O2cj3Oe0A&list=PLrjkTql3jnm8AcFgkc5TE_yQgeHEuKYrG	Available With corresponding faculty

4. Course Prerequisites

SNo	Course Code	Course Name	Module / Topic / Description	Sem	Remarks	Blooms Level
1	17CPL16/26	CPL	Central processing unit and operation	1/2	Basic knowledge about computer hardware	L1
	17PCD13/23	PCD	Knowledge about basic types of data structure	1/2	Different types of data structure	L1
	-	-	Arithmetic Operations with binary representation	-	-	L1

Note: If prerequisites are not taught earlier, GAP in curriculum needs to be addressed. Include in Remarks and implement in B.5.

B. OBE PARAMETERS

1. Course Outcomes

#	COs	Teach. Hours	Concept	Instr Method	Assessment Method	Blooms' Level
-	Student should be able to...	-	-	-	-	-
18cs34.1	Describe the basic structure of Computer, Performance measurement with CPU clock.	05	Operations of computer	Discussions and Readings	Oral question answers and Explain	L2 Understand
18cs34.2	Understand the impact of instruction set architecture on cost-performance of computer design and analyze with various addressing methodologies.	05	Machine instructions structure	Graphic Organizers and Discussion	Analyze and examine and Take home test	L4 Analyzing
18cs34.3	Determine the impact of interrupt on input output devices in the process of interaction between various components.	05	Input output organization and interrupts	Lecture and Readings	Questions are convergent and describe in oral	L2 Understand
18cs34.4	Understand different kind of input output interfaces available for computer system by demonstrations in lab with disassembling of computer.	05	Standard input output interfaces	Discussion and Readings	Oral and describe	L2 Understand
18cs34.5	Determine with the cost-performance issues and design trade-off in designing and constructing a computer processor including memory.	05	Memory System	Readings and Discussion	Student presentations or demonstrations within small groups	L2 Understand
18cs34.6	Describes the virtual memory management and secondary storage devices.	05	Storage devices	Graphic Organizers and Discussion	Analyze and Compare	L4 Analyzing
18cs34.7	Determine the knowledge of designing a logic circuits and apply to computer system.	05	Arithmetic Operations	Demonstrate problem-solving and process for evaluating	Apply the concepts and use to solve the given problems	L3 Applying L5 Evaluating
18cs34.8	Solve the problems in binary representation by using various methods and evaluate with standard circuits.	05	Different methodologies	Demonstrate problem-solving	Practice in multiple contexts	L3 Applying
18cs34.9	Describe the set of hardware simulators to model a complex processor at the behavioral level.	05	Processing unit	Readings and Discussion	Student presentations	L2 Understand
18cs34.10	Determine the current event in the microprocessor research and industry of multiprocessor and embedded systems.	05	Embedded system and large computer system	Readings and Discussion	Student presentations and oral question and answers	L2 Understand

-	**Total**	**50**	-	-	-	-

Note: Identify a max of 2 Concepts per Module. Write 1 CO per concept.

2. Course Applications

SNo	Application Area	CO	Level
1	Understand the basic operations of computer system and learn to calculate the performance of CPU with clock.	CO1	L2
2	Understand the way of writing a machine instructions and then analyze the memory allocation methodologies.	CO2	L4
3	Demonstration of input output organization like accessing I/O devices and handling of interrupt events.	CO3	L2
4	Expose different ways of communicating with I/O devices and standard I/O interfaces.	CO4	L2
5	Acquire the knowledge of semiconductor RAM memories, Static memories, Asynchronous DRAMS, Read only memories.	CO5	L2
6	1. Analyze the memory location by having knowledge of various replacement algorithms. 2. Understand the view of virtual memory and secondary storage devices.	CO6	L4
7	Analyze and design the arithmetic operations and Evaluation of logical circuits.	CO7	L3, L5
8	Apply the knowledge gained on various methodologies.	CO8	L3
9	Understand basic processing unit and organization of simple processor with multiple bus organizations.	CO9	L2
10	Demonstration of various embedded system with different devices and their processor chips to gain the importance of life-long learning.	CO10	L2

Note: Write 1 or 2 applications per CO.

3. Articulation Matrix

(CO – PO MAPPING)

-	Course Outcomes	Program Outcomes												
#	COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	Level
18cs34.1	Describe the basic structure of Computer, Performance measurement with CPU clock.	2	2	3	1			2					1	L2
18cs34.2	Understand the impact of instruction set architecture on cost-performance of computer design and analyze with various addressing methodologies.	2	2	3	2		1	2					2	L4
18cs34.3	Determine the impact of interrupt on input output devices in the process of interaction between various components.	2	2	1	2	1							1	L2
18cs34.4	Understand different kind of input output interfaces available for computer system by demonstrations in lab with disassembling of computer.	2	1	3	1			2					2	L2
18cs34.5	Determine with the cost-performance issues and design trade-off in designing and constructing a computer processor including memory.	2	2	2	1	1							2	L2
18cs34.6	Describes the virtual memory management and secondary storage devices.	2	2	3				2				2	2	L4
18cs34.7	Determine the knowledge of designing a logic circuits and apply to computer system.	2	2		2		2	2					3	L3, L5
18cs34.8	Solve the problems in binary representation by using various methods and evaluate with standard circuits.	3	2	3	2								2	L3
18cs34.9	Describe the set of hardware simulators to model a complex processor at the behavioral level.	2	2	1		2		2					3	L2
18cs34.10	Determine the current event in the microprocessor research and industry of multiprocessor and embedded systems.	3	3	3	2	2							2	L2
	Avg CO	2	2	3	2	2	2	2				2	2	
Note: Mention the mapping strength as 1, 2, or 3														

4. Mapping Justification

Mapping		Justification	Mapping Level
CO	**PO**	**-**	**-**
CO1	PO1	Knowledge of basic structure of computer is needed to build a complex circuits.	L2
CO1	PO2	Analyze the performance of the CPU with different processor.	L3
CO1	PO3	Processes the performance of the computer to provide solutions for complex problems.	L4
CO1	PO4	Analyze the different performance values with standard reference values.	L3
CO1	PO7	Understand the impact of different uses of the computer and demonstrate the knowledge to find the solutions.	L2
CO1	PO12	Identify new technology to solve various complex problems of the computer.	L2
CO2	PO1	Apply the knowledge of computer designing and cost performance for implementing various methodologies for instruction set architecture.	L4
CO2	PO2	Identify the proper methodology to over come a various problems of implementing an optimized solution for different instruction sets.	L2
CO2	PO3	Processes the complex instruction set architecture to produce the solution that meets the cost-performance of the computer.	L4
CO2	PO4	Analyze the cost performance and various addressing methodologies to provide a solution for complex solutions.	L4
CO2	PO6	Apply the reasoning for cost performance of various architecture and their uses.	L4
CO2	PO7	Understand the impact in societal and find the solutions according to environmental contexts.	L2
CO2	PO12	Information acquired from the fundamental of instruction set architecture provides lifelong learning in the context of technological change.	L2
CO3	PO1	Apply the evaluation of different hardware components associated with the input-output organization of a computer.	L5
CO3	PO2	Analysis of interaction of Input and output with processing unit on various operation.	L4
CO3	PO3	Design a system components in such a way that the performance speed should get increase.	L5
CO3	PO4	Investigate the different design of a system components and design an optimized solutions.	L4
CO3	PO5	Understand the modern tools and technique and apply that to overcome a limitation of complex engineering activities.	L2
CO3	PO12	Recognize the need in designing of various input-output devices.	L2
CO4	PO1	Knowledge about the various device interfaces of the computer hardware.	L2
CO4	PO2	Identify the interfaces available for input and output devices and analyze the different hardware components which uses these interfaces to communicate with processor.	L2
CO4	PO3	Processes the system components that meets the appropriate need in performing various operations.	L4
CO4	PO4	Analysis of different kind of interfaces which are available for various input output devices.	L4
CO4	PO7	Demonstrate the components of the computer by disassembling the system to understand the interfaces.	L3
CO4	PO12	Information acquired from the different kind of I/O interfaces which requires lifelong learning in the context of technological change.	L2
CO5	PO1	Knowledge of memory storage to give the solution for various complex data storage issues.	L2
CO5	PO2	Identify the problems in data storage and analyze the substantiated	L2

		conclusion using engineering research.	

CO5	PO3	Design a solution for handling the memory management for storing large amount of data in the system.	L6
CO5	PO4	Analysis of available memory spaces in the system in designing and constructing a computer processors.	L4
CO5	PO5	Understand the latest techniques and the current need in handling data in memory storage.	L2
CO5	PO12	Identify the new technologies to evolve the future use of the memory devices.	L2
CO6	PO1	Knowledge about memory management to give implement a virtual memory space in existing device.	L2
CO6	PO2	Analyze the problem of memory management and identify the solution by implementing virtual-memory spaces in the same system.	L4
CO6	PO3	Design the virtual-memory architecture to manage the available memory space in the storage of large data.	L4
CO6	PO7	Understand the impact on current system memory while implementing a virtual memory space in the same system.	L2
CO6	PO11	Apply the techniques to create virtual memory spaces to manage projects in multidisciplinary environments.	L5
CO6	PO12	Ability to cop up with different methodologies to create a virtual-memory space after learning the memory management schemes.	L 2
CO7	PO1	Knowledge about the basic logical gates for designing a complex architecture for system operations.	L2
CO7	PO2	Identify the various techniques for designing a logic circuits for different computation.	L2
CO7	PO4	Investigate and analyze the circuits based on complexity of the operation.	L4
CO7	PO6	Apply the methodologies in a proper manner so that computation should not lead to wrong output.	L4
CO7	PO7	Demonstrate the complex calculations solutions by implementing a optimized logic circuits.	L3
CO7	PO12	Performing mathematical operation in computer requires the performance issue when it comes to large data so life-long learning is needed in designing optimized logical circuits.	L2
CO8	PO1	Knowledge of basic conversions is required to convert complex calculations into machine understand format.	L2
CO8	PO2	Identify the optimized method to perform a various mathematical operations in short time.	L2
CO8	PO3	Design the optimized circuits for complex problem-solving in the system.	L5
CO8	PO4	Analyze the various methods for conversion of numerical values into machine understandable form and evaluate the operation with standard circuits.	L4
CO8	PO12	Information acquired from the number representation and standard circuits which provides lifelong learning in the context of technological change.	L2
CO9	PO1	Knowledge of basic components of computer and instructions execution in the processor.	L2
CO9	PO2	Identify the complexity of the current methods and analyze the system operations at a behavioral level of the system.	L2
CO9	PO3	Design the set of hardware simulators for complex problems of the processor.	L5
CO9	PO5	Select modern simulation tools for developing a optimized solution for processor operation management	L2
CO9	PO7	Understand the impact of the hardware devices connected to the system and the need for developing more sustainable technique.	L1
CO9	PO12	Recognize the future enhancement needed for solving a various	L2

		problems in the computer world.	
CO10	PO1	Knowledge of current events and techniques using with microprocessor to build a solution for complex operations.	L2
CO10	PO2	Analyze the various current microprocessor technologies which are using in a different industries and identify the required solution for developing new methodologies.	L2
CO10	PO3	Design system components for implementing automatic embedded system for home appliances and more.	L4
CO10	PO4	Investigate the current research and analyze the improvements that are needed in the multiprocessing system.	L5
CO10	PO5	Understand the current technologies which are available and the limitation to overcome complexity in the system.	L4
CO10	PO12	Identify the broadest contexts of technological changes in the multi-core processor and in embedded system.	L2

Note: Write justification for each CO-PO mapping.

5. Curricular Gap and Content

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					
3					
4					
5					

Note: Write Gap topics from A.4 and add others also.

6. Content Beyond Syllabus

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					

Note: Anything not covered above is included here.

C. COURSE ASSESSMENT

1. Course Coverage

Module #	Title	Teaching Hours	No. of question in Exam						CO	Levels
			CIA-1	CIA-2	CIA-3	Asg	Extra Asg	SEE		
1	Basic structure of computer	10	2	-	-	1	1	2	CO1, CO2	L2, L4
2	Input/output Organization	10	2	-	-	1	1	2	CO3, CO4	L2
3	Memory system	10	-	2	-	1	1	2	CO5, CO6	L2, L4
4	Arithmetic operations	10	-	2	-	1	1	2	CO7, Co8	L3,L5
5	Basic processing unit and Embedded system	10	-	-	4	1	1	2	CO9, CO10	L2
-	**Total**	**50**	**4**	**4**	**4**	**5**	**5**	**10**	-	-

Note: Distinct assignment for each student. 1 Assignment per chapter per student. 1 seminar per test per student.

2. Continuous Internal Assessment (CIA)

Evaluation	Weightage in Marks	CO	Levels
CIA Exam – 1	30	CO1, CO2, CO3, CO4	L2, L4
CIA Exam – 2	30	CO5, CO6, CO7, Co8	L2, L3, L4,L5
CIA Exam – 3	30	CO9, CO10	L2
Assignment - 1	10	CO1, CO2, CO3, CO4	L2, L4
Assignment - 2	10	CO5, CO6, CO7, CO8	L2, L3, L4,L5
Assignment - 3	-	CO9, CO10	L2
Seminar - 1	-	CO1, CO2, CO3, CO4	L2, L4
Seminar - 2	-	CO5, CO6,CO7,CO8	L2, L3, L4,L5
Seminar - 3	10	CO9, CO10	L2
Other Activities – define – Slip test		CO1 to Co9	L2, L3, L4
Final CIA Marks	**40**	**-**	**-**

Note : Blooms Level in last column shall match with A.2 above.

D1. TEACHING PLAN - 1

Module - 1

Title:	Basic structure of computer	Appr Time:	16 Hrs
a	***Course Outcomes***	-	**Blooms**
-	The student should be able to:	-	**Level**
1	Describe the basic structure of Computer, Performance measurement with CPU clock.	CO1	L2
2	Understand the impact of instruction set architecture on cost-performance of computer design and analyze with various addressing methodologies.	CO2	L4
b	***Course Schedule***	-	-
Class No	**Module Content Covered**	**CO**	**Level**
1	Basic Operational Concepts	Co1	L2
2	Bus Structures	Co1	L2
3	Processor Clock	Co1	L2
4	Basic Performance Equation	Co1	L2
5	CPU Clock Rate	Co1	L2
6	Performance Measurement	Co1	L2
7	Machine Instructions and Programs	Co2	L2
8	Memory Location and Addresses	Co2	L2
9	Memory Operations	Co2	L2
10	Instructions and Instruction Sequencing.	Co2	L4
11	Addressing Modes	Co2	L4
12	Assembly Language	Co2	L4
13	Basic Input and Output Operations	Co2	L2
14	Stacks and Queues, Subroutines	Co2	L2
15	Additional Instructions	Co2	L3
16	Encoding of Machine Instructions	Co2	L2
c	**Application Areas**	**CO**	**Level**
1	Use of the various operations of computer system and learn to calculate the performance of CPU with clock.	CO1	L2
2	Used in addressing a memory location in computer system.	CO2	L4
d	**Review Questions**	-	-
1	With the neat diagram explain different processor register? List the steps needed to execute the machine instruction.	CO1	L2
2	Explain briefly about performance evaluation by using various bench marks.	CO1	L2
3	Draw the basic functional units of a computer.	CO1	L2
4	Explain the operations of stacks and queues.	CO2	L4
5	Discuss about different types of addressing modes.	CO2	L4
6	Explain the operations of stacks and queues.	CO2	L4
7	Give the difference between RISC and CISC.	CO2	L2
8	Write an algorithm for the division of floating point number and illustrate with an example.	CO2	L2
9	Explain BIG-ENDIAN and LITTLE-ENDIAN methods of byte addressing with proper exaple.	CO1	
10			
11			
e	**Experiences**	-	-
1		CO1	L2
2			
3			
4		CO3	L3

5			

Module – 2

Title:	Input/output Organization	Appr Time:	10 Hrs
a	***Course Outcomes***	-	**Blooms**
-	The student should be able to:	-	**Level**
1	Determine the impact of interrupt on input output devices in the process of interaction between various components.	CO3	L2
2	Understand different kind of input output interfaces available for computer system by demonstrations in lab with disassembling of computer.	CO4	L2
b	***Course Schedule***	-	-
Class No	**Module Content Covered**	**CO**	**Level**
17	Input/Output Organization: Accessing I/O Devices	Co3	L2
18	Interrupts – Interrupt Hardware	Co3	L2
19	Enabling and Disabling Interrupts	Co3	L2
20	Handling Multiple Devices	Co3	L2
21	Controlling Device Requests	Co3	L2
22	Exceptions	Co3	L2
23	Direct Memory Access	Co3	L2
24	Buses Interface Circuits	Co4	L2
25	Standard I/O interfaces: PCI BUS, SCSI BUS, USB.	Co4	L2
c	**Application Areas**	**CO**	**Level**
1	Use to Demonstrate of input output organization like accessing I/O devices and handling of interrupt events.	CO3	L2
2	Expose different ways of communicating with I/O devices and standard I/O interfaces.	CO4	L2
d	**Review Questions**	-	-
12	The input status bit in an interface-circuit is cleared as soon as the input data register is read. Why is this important?	CO3	L1
13	What is the difference between a subroutine and an interrupt-service routine?	CO4	L3
14	Consider a computer in which several devices are connected to a common interrupt-request line. Explain how you would arrange for interrupts from device j to be accepted before the execution of the interrupt service routine for device i is completed. Comment in particular on the times at which interrupts must be enabled and disabled at various points in the system.	CO3	L2
15	Consider the daisy chain arrangement. Assume that after a device generates an interrupt-request, it turns off that request as soon as it receives the interrupt acknowledge signal. Is it still necessary to disable interrupts in the processor before entering the interrupt service routine? Why?	CO4	L4
16	Describe the operation of synchronous and asynchronous bus.	CO4	L2
17	Discuss the features of parallel and serial interface techniques.	CO3	L5
18	Describe how a read operation is performed in PCI bus.	CO3	L2
19	Explain how USB operates with split-traffic mode.	CO3	L3
e	**Experiences**	-	-
1		CO1	L2
2			
3			
4		CO3	L3
5			

E1. CIA EXAM – 1

a. Model Question Paper - 1

Crs Code:	18cs34	Sem:	III	Marks:	30	Time:	75 minutes		
Course:	Computer Corganization								
-	**-**	**Note: Answer any 3 questions, each carry equal marks.**					**Marks**	**CO**	**Level**
1	a	With neat diagram, discuss basic operational concepts of a computer.					20	CO1	L1
	b	Write the difference between RISC and CISC processor						CO1	L2
	c	Define addressing modes. Explain the following addressing modes with an example for each i) Index addressing ii) Indirect addressing mode iii) Relative addressing mode iv) Auto decrement addressing mode.						CO2	L4
2	a	Discuss briefly encoding of machine instruction.					20	Co2	L2
	b	A program contain 1000 instruction out of that 25% instructions requires 4 clock cycles. 40% instruction requires 5 clock cycles and remaining 3 clock cycles for execution. Find the total time required to execute the program running in 1GHz machine.						Co2	L4
	c	Explain different Rotate instructions.						Co2	L3
	d	Write an ALP program to copy 'N' numbers from array 'A' to array 'B' using direct addresses. (Assume A and B are starting memory locations of an array)						Co2	L2
3	a	With neat diagram describe the input output operations.					20	Co3	L1
	b	With neat sketches, explain various methods for handling multiple interrupt requests.							L2
	c	With neat diagram, explain in detail the input interface circuit.						Co4	L1
	d	Define Bus Arbitration. Explain any one approach of bus arbitration.							L2
4	a	Write a note on register in DMA interface.					20		L2
	b	With a block diagram explain how the printer interfaced to processor.							L2
	c	Explain the following with respect to U.S.B i) U.S.B Architecture ii) U.S.B protocols							L1

b. Assignment -1

Note: A distinct assignment to be assigned to each student.

Model Assignment Questions

Crs Code:	18cs34	Sem:	III	Marks:		Time:	90 – 120 minutes
Course:	Computer Organization						

Note: Each student to answer 2-3 assignments. Each assignment carries equal mark.

SNo	USN	Assignment Description	Marks	CO	Level
1		What is bus? Explain single bus and multiple bus structure used to interconnect functional units in computer system.	8	CO1	L2
2		Explain how the performance of the computer can measured?	5	CO1	L2
3		Explain byte address ability mention the two ways that byte addresses can be assigned across the word with proper example.		CO2	L4
4		What is an addressing mode? Explain different generic addressing modes with an example for each.	5	CO2	L4
5		What are assembler directives? Explain any two directives.		CO2	L4
6		Explain with neat diagram I/O interface for an input device.		Co3	L2
7		Explain the following: 1) Interrupt concept 2) interrupt hardware.		Co3	L2
8		Explain different interrupt Enabling and Disabling methods. List the sequence of events involved in handling an interrupt request from a single device.		Co3	L4
9		With neat block diagram, Explain different methods of handling multiple I/O devices.		Co3	L3
10		Define exception. Explain kinds of exceptions?		Co3	L2
11					
12					
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D2. TEACHING PLAN - 2

Module – 3

Title:	Memory system	Appr Time:	16 Hrs
a	***Course Outcomes***	-	**Blooms**
-	The student should be able to:	-	**Level**
1	Determine with the cost-performance issues and design trade-off in designing and constructing a computer processor including memory.	CO5	L2
2	Describes the virtual memory management and secondary storage devices.	CO6	L3
b	***Course Schedule***		
Class No	**Module Content Covered**	**CO**	**Level**
1	Memory System: Basic Concepts	C5	L2
2	Semiconductor RAM Memories	C5	L2
3	Read Only Memories	C5	L2
4	Speed, Size, and Cost	C5	L2
5	Cache Memories – Mapping Functions	C5	L2
6	Replacement Algorithms	C5	L4
7	Performance Considerations	C6	L4
8	Virtual Memories	C6	L2
9	Secondary Storage.	C6	L2
c	**Application Areas**	**CO**	**Level**
1	Acquire the knowledge of semiconductor RAM memories, Static memories, Asynchronous DRAMS, Read only memories.	CO5	L3
2	1. Analyze the memory location by having knowledge of various replacement algorithms. 2. Understand the view of virtual memory and secondary storage devices.	CO6	L4
d	**Review Questions**	-	-
1	Consider the dynamic memory cell. Assume that C = 30 femtofarads (10^{-15} F) and that leakage current through the transistor is about 0.25 picoamperes (10^{-12} A). The voltage across the capacitor when it is fully charged is 1.5 V. The cell must be refreshed before this voltage drops below 0.9 V. Estimate the minimum refresh rate.	CO5	L2
2	Give a critique of the following statement: "Using a faster processor chip results in a corresponding increase in performance of a computer even if the main-memory speed remains the same."	CO5	L4
3	The cache block size in many computers is in the range of 32 to 128 bytes. What would be the main advantages and disadvantages of making the size of cache blocks larger or smaller?	CO5	L2
4	In a computer with a virtual-memory system, the execution of an instruction may be interrupted by a page fault. What state information has to be saved so that this instruction can be resumed later? Note that bringing a new page into the main-memory involves a DMA transfer, which requires execution of other instructions. Is it simpler to abandon the interrupted instruction and completely re-execute it later? Can this be done?	CO6	L2
5	Magnetic disks are used as the secondary storage for program and data files in most virtual-memory systems. Which disk parameter(s) should influence the choice of page size?	CO6	L2
6	A disk unit has 24 recording surfaces. It has a total of 14,000 cylinders. There is an average of 400 sectors per track. Each sector contains 512 bytes of data. i) What is the maximum number of bytes that can be stored in this unit ? ii) What is the data-transfer rate in bytes per second at a rotational speed of 7200 rpm? iii) Using a 32-bit word, suggest a suitable scheme for specifying the disk address.	CO6	L4

7	Discuss the main features of SDRAM with a neat diagarm.	CO6	L2
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e	**Experiences**	-	-
1		CO5	L2
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4		CO6	L4
5			

Module – 4

Title:	Arithmetic operations	Appr Time:	16 Hrs
a	***Course Outcomes***	-	**Blooms**
-	The student should be able to:	-	**Level**
1	Determine the knowledge of designing a logic circuits and apply to computer system.	CO7	L2
2	Solve the problems in binary representation by using various methods and evaluate with standard circuits.	CO8	L3
b	***Course Schedule***		
Class No	**Module Content Covered**	**CO**	**Level**
1	Arithmetic: Numbers		
2	Arithmetic Operations and Characters		
3	Addition and Subtraction of Signed Numbers		
4	Design of Fast Adders		
5	Multiplication of Positive Numbers		
6	Signed Operand Multiplication		
7	Fast Multiplication		
8	Integer Division,		
9	Floating-point Numbers and Operations.		
c	**Application Areas**	**CO**	**Level**
1	Analyze and design the arithmetic operations and Evaluation of logical circuits.	CO8	L3
2	Apply the knowledge gained on various methodologies.	CO7	L4
d	**Review Questions**	-	-
1	Represent the decimal values 5, -2, 14, -10, 26, -19, 51 and -43 as signed 7-bit numbers in the following binary formats: sign-and-magnitude 1's-complement 2's-complement	CO7	L3
2	Given A=10101 and B=00101, perform A/B using non-restoring division algorithm.	CO7	L3
3	Represent 1259.12510 in single precision and double precision formats	CO8	L2
4	Represent the following decimal numbers using IEEE standard floating point notation. i) +1.725 ii)-25.125 iii)-0.08125 iv) +45	CO7	L3
5	Show the sequential multiplication process for each of the following pairs of numbers. X is multiplier and Y is multiplicand. i) X = 0101, Y = 1101 ii) X = 1110, Y = 0111	CO8	L2
6	Design BCD adder for adding 2 decimal digits using 4-bit binary adder and external logic gates. The inputs are A = A3 A2 A1 A0 and B = B3 B2 B1 B0 and a carry-in, cin bit. The range of A and B is from 0 to 9.	CO8	L3
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e	**Experiences**	-	-
1		CO7	L2
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4		CO8	L3
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E2. CIA EXAM – 2

a. Model Question Paper - 2

Crs Code:	CS501PC	Sem:	I	Marks:	30	Time:	75 minutes		
Course:	Design and Analysis of Algorithms								
-	**-**	**Note: Answer any 2 questions, each carry equal marks.**					**Marks**	**CO**	**Level**
1	a	Draw a diagram and explain the working of 16MB DRAM chip configured as 2M * 8					20	CO5	L1
	b	Describe organization of a 2M * 32 memory using 512k * 8 memory chips.						CO5	L2
	c	Explain Associative mapping technique and set Associative mapping technique.						CO6	L3
	d	Define: i) Memory latency ii) Memory bandwidth iii) Hit rate iv) Miss penalty.						CO6	L1
2	a	What is virtual memory? With a diagram explain how virtual memory address is translated.					20	CO7	L2
	b	Write a note on: i) Magnetic tape system ii) Flash memory.							L4
	c	A Block-set associative cache consist of a total of 64 blocks divided into 4-blocks sets. The main memory contains 4096 blocks, each consisting of 128 words. i) How many bits are there in main memory address? ii) how many bits are there in each of the TAG, SET and WORD fields?						CO7	L3
	d	Define the following with respect to cache memory: i) Valid bit ii) dirty bit iii) Stale data iv) Flash the cache.						CO7	L2
3	a	Convert the following pairs of decimal numbers to 5-bit signed 2's compliment binary numbers and add them. State whether or not overflow occurs in each case. i) 5 and 10 ii) -14 and 11 iii) -5 and 7 iv) -10 and -13					20	CO8	L3
	b	Design the 16 bit carry look ahead adder using 4-bit adder. Also unite the expression for C_{i+1}						CO8	L4
	c	Draw the two n-bit number X and Y to perform addition/subtraction.						CO8	L3
	d	Explain the concept of carry save addition for the multiplication operation, M * Q = P for 4-bit operand with diagram and suitable example.						CO8	L2
4	a	Multiply each of the following pairs of signed 2's compliment number using the booth algorithm.(A = multiplicand and B= multiplier) i) A= 010111 B = 110110 ii) A = 110011 and B = 101100 iii) A = 110101 and B = 011011 iv) A = 001111 and B = 001111					20		L3
	b	Perform division operation on the following unsigned numbers using the restoring method. Dividend = (10101)2 Divisor = (00100)2							L3
	c	With a neat diagram, explain the floating point addition/subtraction unit.							L2
	d	Explain an n bit ripple carry adder with neat block diagram.							L3

b. Assignment – 2

Note: A distinct assignment to be assigned to each student.

Model Assignment Questions

Crs Code:	18cs34	Sem:	III	Marks:		Time:	90 – 120 minutes
Course:	Computer Organization						

Note: Each student to answer 2-3 assignments. Each assignment carries equal mark.

SNo	USN	Assignment Description	Marks	CO	Level
1		Explain connection between memory and processor with memory read and write operations?	5	CO5	L2
2		Draw the organization of 1Kx1 memory cell and explain its working.	5	CO5	L2
3		Write briefly about read only memories and Flash memory's.		CO5	L4
4		Draw the organization of a 16x memory chip and explain its working.	5	CO6	L2
5		What is refreshing? Explain the concept of refreshing in dynamic memory?		CO6	L2
6		With a neat diagram explain the virtual memory organization.		CO7	L3
7		What is virtual memory? With a diagram explain how virtual memory address is translated.		CO7	L2
8		With a neat diagram explain the translation of virtual address to a physical address?		CO7	L4
9		Explain the 4-bit carry look ahead adder.		CO8	L3
10		Design a logic circuit to perform addition and subtraction of two 'n' numbers X and Y.		CO8	L2
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D3. TEACHING PLAN - 3

Module – 5

Title:	Basic processing unit and Embedded system	Appr Time:	16 Hrs
a	***Course Outcomes***	-	**Blooms**
-	The student should be able to:	-	**Level**
1	Describe the set of hardware simulators to model a complex processor at the behavioral level.	CO9	L2
2	Determine the current event in the microprocessor research and industry of multiprocessor and embedded systems.	CO10	L2
b	***Course Schedule***		
Class No	**Module Content Covered**	**CO**	**Level**
1	Basic Processing Unit: Some Fundamental Concepts	CO9	L2
2	Execution of a Complete Instruction	CO9	L2
3	Multiple Bus Organization	CO9	L2
4	Hard-wired Control	CO9	L2
5	Micro programmed Control	CO9	L2
6	Pipe lining	CO9	L2
7	Embedded Systems and Large Computer Systems: Basic Concepts of pipe lining	CO10	L2
8	Examples of Embedded Systems	CO10	L2
9	Processor chips for embedded applications	CO10	L2
10	Simple Micro controller	CO10	L2
11	The structure of General-Purpose Multiprocessors	CO10	L2
c	**Application Areas**	**CO**	**Level**
1	Understand basic processing unit and organization of simple processor with multiple bus organizations.	CO9	L2
2	Demonstration of various embedded system with different devices and their processor chips to gain the importance of life-long learning.	CO10	L2
d	**Review Questions**	-	-
1	Why is the Wait-for-memory-function-completed step needed for reading from or writing to the main memory?	CO10	L1
2	For the single bus organization, write the complete control sequence for the instruction: Move (R1), R1	CO10	L3
3	Write the sequence of control steps required for the single bus organization in each of the following instructions: Add the immediate number NUM to register R1. Add the contents of memory-location NUM to register R1. Add the contents of the memory-location whose address is at memory-location NUM to register R1. Assume that each instruction consists of two words. The first word specifies the operation andN the addressing mode, and the second word contains the number NUM	CO9	L2
4	Show the control steps for the Branch on Negative instruction for a processor with three-bus organization of the data path	CO9	L4
5	With block diagram, explain NUMA multiprocessor.	CO10	L2
6	Write a short not on home telemetry.	CO10	L2
7	With block diagram, explain operation of counter/timer.	CO10	L2
8	With block diagram, explain operation of microcontroller chips.	CO10	L3
9	With block diagram, explain serial I/O interface. Also, explain serial interface register	CO9	L4
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e	**Experiences**	-	-

1		CO10	L2
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4		CO9	L3
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E3. CIA EXAM – 3

a. Model Question Paper - 3

Crs Code:	CS501PC	Sem:	I	Marks:	30	Time:	75 minutes		
Course:	Design and Analysis of Algorithms								
-	**-**	**Note: Answer any 2 questions, each carry equal marks.**					**Marks**	**CO**	**Level**
1	a	Discuss with neat diagram, the single bus organization of the data path inside a processor.					20	CO9	L1
	b	Write the sequence of control steps required for single bus structure for each if the following instructions. i) Add the contents of memory location NUM to register R1. ii) Add the contents of memory location whose address is at memory location NUM to register R1.							L2
	c	Explain with neat diagram micro-programmed control method for design of control unit and write the micro-routine for the instruction Branch < 0.						CO9	L3
	d	Draw and explain multiple bus organization of CPU and write the control sequence for the instruction Add R4, R5, R6 for the multiple bus organization.							
2	a	With block diagram explain the working of microwave oven in an embedded system.					20	CO10	L2
	b	With block diagram explain parallel I/O interface.							L4
	c	Discuss digital camera with neat block diagram.							L3
3	a						20	CO10	L1
	b							CO10	L2
	c								L1
	d								L2
4	a						20		L2
	b								L2
	c								L1
	d								L3

b. Assignment – 3

Note: A distinct assignment to be assigned to each student.

Model Assignment Questions

Crs Code:	CS501PC	Sem:	I	Marks:	5 / 10	Time:	90 – 120 minutes
Course:	Design and Analysis of Algorithms						

Note: Each student to answer 2-3 assignments. Each assignment carries equal mark.

SNo	USN	Assignment Description	Marks	CO	Level
1		Write down the control sequence for the instruction Add R4, R5, R6 for three-bus organization.	5	CO9	L2
2		With a neat sketches explain the organization of a micro programmed control unit.?	5	CO9	L3
3		With a diagram explain typical single bus processor data path?		CO10	L4
4		Differentials hardwired and micro programmed control unit?	5	CO10	L3
5		Explain the process of fetching a word from memory with diagram?			
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F. EXAM PREPARATION

1. University Model Question Paper

Course:	Design and Analysis of Algorithms					Month / Year	June /2018
Crs Code:	18cs34	Sem:	III	Marks:	100	Time:	180 minutes

-	Note	Answer all FIVE full questions. All questions carry equal marks.	Marks	CO	Level
1	a	Define Addressing Mode. Give the details of different addressing modes.	16 / 20	CO1	L2
	b	Describe the basic operational concepts between the processor and memory.		CO2	L2
		OR			
-	a	What is Subroutine? How to pass parameters to subroutines? Illustrate with an example	16 / 20	CO1	L2
	b	How to encode assembly instructions into 32-bit words? Explain with examples.		CO2	L4
2	a	Define Bus Arbitration. With diagrams, explain the centralized bus arbitration mechanism.	16 / 20	CO3	L2
	b	With the help of timing diagram, briefly discuss the main phases of SCSI bus involved in its operation.		CO4	L2
		OR			
-	a	With neat diagrams, explain how to interface printer to the processor.	16 / 20	CO3	L2
	b	Explain the following methods of handling interrupts from multiple devices. i) Interrupt nesting/priority structure ii) Daisy chain method.		CO4	L2
3	a	Describe how to translate virtual address into physical address with diagram.	16 / 20	CO5	L2
	b	Draw and explain the internal organisation of 2M x 8 asynchronous DRAM chip.		CO6	L2
		OR			
-	a	Describe any two mapping functions in cache.	16 / 20	CO5	L2
	b	Describe the principles of magnetic disk.		CO6	L2
4	a	form the operations on 5 — bit signed numbers using 2's complement system. Also indicate whether overflow has occurred. i) (-10) + (-13) ii) (-10) — (-13) iii) (-2) + (-9).	16 / 20	CO7	L3
	b	Perform the multiplication of 13 and -6 using Booth algorithm and Bit-pair recording method.		CO8	L3
		OR			
-	a	Perform the restoring division for 8/3 by showing all the steps	16 /	CO7	L3

			20		
	b	Explain the logic diagram of 4 — bit carry look ahead adder and its operations.		CO8	L2
5	a	Draw and explain multiple bus organization along with its advantages.	16 / 20	CO9	L2
	b	Write down the control sequence for the instruction Add (R3) , R1 for single bus organization		CO10	L3
		OR			
	a	With block diagram, explain the general requirements and working of digital camera.	16 / 20	CO9	L2
	b	Write the control sequence for an unconditional branch instruction.		C010	L2

2. SEE Important Questions

Course:	Design and Analysis of Algorithms					Month / Year	June /2018
Crs Code:	18CS34	Sem:	III	Marks:	100	Time:	180 minutes

	Note	Answer all FIVE full questions. All questions carry equal marks.	-	-	
Module	Qno.	Important Question	**Marks**	**CO**	**Year**
1	1	With neat diagram explain simple I/O operations involving in keyboard and display device.	16 / 20	Co1	2018
	2	Define subroutine. Explain subroutine linkage using a link register and stack frame.		Co1	2017
	3	Explain different parameter passing technique with usage of stack in nested subroutine calls.		Co1	2015
	4	Explain different shift and rotate instructions with proper examples.		Co2	2015
	5	Explain encoding of machine instruction into 32-bit word.		Co2	2016
2	1	What is necessity of DMA controller? Explain (1) Cycle stealing (2) Burst mode.	16 / 20	Co3	2017
	2	Show the possible register configurations in DMA interface, Explain direct memory access(DMA)		Co3	2018
	3	What is necessity of BUS Arbitration? Explain different methods of bus arbitration.		Co4	2017
	4	Define BUS? Explain with neat detailed timing diagram for the input transfer using multiple clock cycle of synchronous Bus?		Co4	2016
	5	Explain with neat detailed timing diagram for handshake control of data transfer during an output operation.		Co4	2015
3	1	Explain the working of 16MB DRAM chip configured as 1M*16 (2M*8) memory chip.	16 / 20	Co5	2015
	2	Define: i) Memory latency ii) Memory bandwidth iii) Hit rate iv) Miss penalty.		Co5	2016
	3	With diagram explain different types of memory's with speed, cost and size.		Co5	2017
	4	Define cache memory? Explain different cache mapping functions.		Co5	2018
	5	Explain the features of memory design that leads to improved performance of computer.		Co6	2015
4	1	Given A=10101 and B=00100, Perform A/B using restoring division algorithms.	16 / 20	Co7	2016
	2	Perform signed multiplication of numbers (-12) and (-11) using Booth's algorithm.		Co7	2016
	3	Design 4-bit carry look ahead logic and explain how it is faster than 4-bit ripple adder.		Co7	2017
	4	Explain normalization, excess-exponent and special values with respect to IEEE floating point representation.		Co8	2018
	5	Perform the following operations on the 5-bit signed numbers using 2's compliment representation system. Also indicate whether overflow has occurred i) (-10) + (-13) ii) (-10) - (+4) iii) (-3) + (-8) iv) (-10) - (+7)		Co8	2014
5	1	Write and explain the control sequences for the execution of an unconditional branch instruction.	16 / 20	Co9	2015
	2	Draw and explain the multi-bus organization of the data path inside a processor?		Co9	2016
	3	What is embedded system? Explain with examples.		Co10	2015
	4	Explain with neat diagram structure of general purpose multiprocessor?		Co10	2018
	5				2017